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**DIV: B**

**TOPIC:** DE

**Experiment Number:** 8

**DATE:**

**Aim** : To realize asynchronous 3-bit Up Counter.

**Equipment's** : Breadboard, IC 7474(D flip flop), CRO, Function Generator, wires (for connection), LED board, Power Supply.

**Theory :**

A [Counter](https://en.wikipedia.org/wiki/Counter_(digital)) is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2… .They can also  be designed with the help of flip flops. They are used as frequency dividers where the frequency of given pulse waveform is divided. Counters are sequential circuit that count the number of pulses can be either in binary code or BCD form. The main properties of a counter are timing , sequencing , and counting. Counter  works in two modes :

Up counter (An up-counter counts events in increasing order),

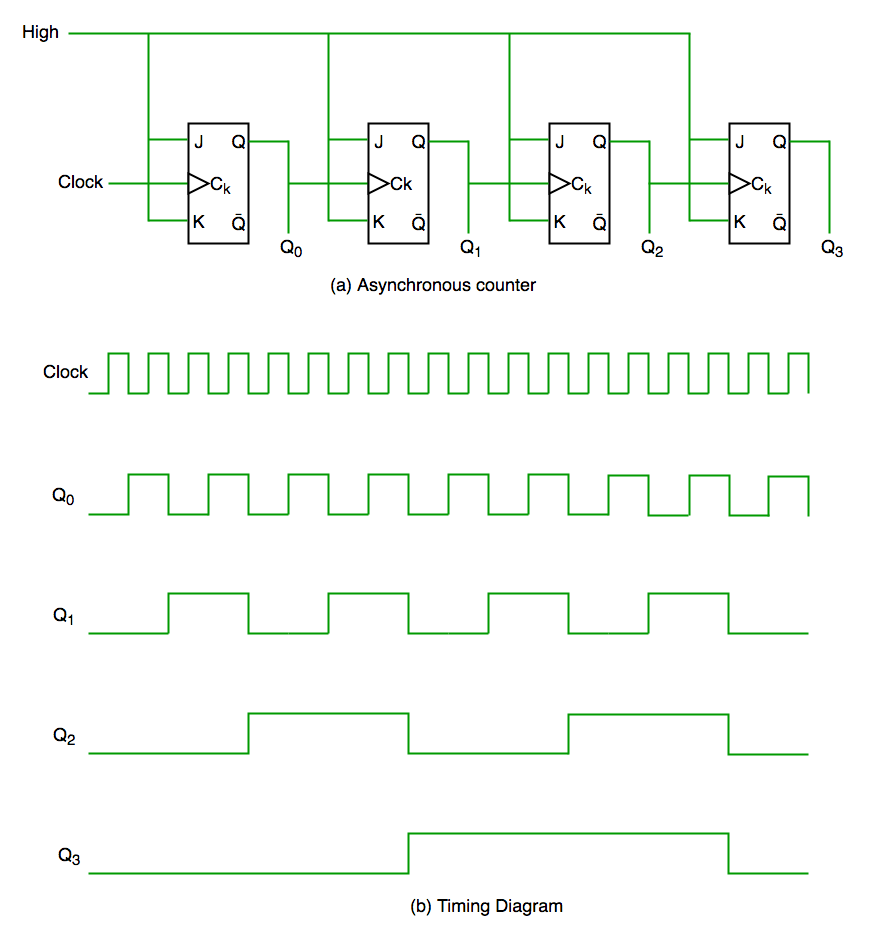
Down counter(A down-counter counts stuff in the decreasing order)

Counters are broadly divided into two categories:

1. **Asynchronous Counter**

In asynchronous counter we don’t use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following flip flop is driven by output of previous flip flops.It is evident from timing diagram that Q0 is changing as soon as the rising edge of clock pulse is encountered, Q1 is changing when rising edge of Q0 is encountered(because Q0 is like clock pulse for second flip flop) and so on. In this way ripples are generated through Q0,Q1,Q2,Q3 hence it is also called RIPPLE counter. A ripple counter is a cascaded arrangement of flip flops where the output of one flip flop drives the clock input of the following flip flop .

Following diagram of asynchronous counter :



**2) Synchronous Counter**

Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel. The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

As our is focusing on asynchronous counters we studied them broadly.

Now as we know there are two types of counter up and down, so we now study about asynchronous up counters

Asynchronous Up Counters

Up counters which work on Asynchronous method are asynchronous up counters. We can design different types of counter depending on asynchronous, synchronous, up, down, also depending on the bit(2-bit,3-bit, 4-bit…), also depending on the flip flops are used in the counter as there two types of flip flop rising edge and falling edge and because of this many variation can be designed in counters.

Now in our journal we are going to discuss about *asynchronous 3 bit up Counter* .

For asynchronous 3 bit up counter 3 flip flops are used each flip flop corresponding to each bit from 0 to 7 so there are 8 count states (000, 001, 010, 011, 100, 101, 110, 111)

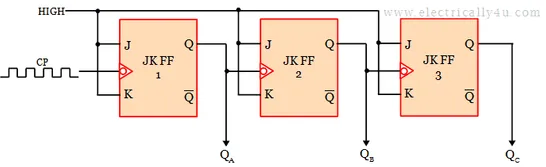
So counter start from 0 then goes up-to 7 and then comebacks to 0 and counts till 7 this process goes on in loop.

This counter can be of two types depending on the flip flop whether it is falling edge or rising edge.

**Using JK flip flop**

**Asynchronous 3 bit up counter [Falling edge flip flop] :**

Here falling edge flip flop are used to design a up counter .

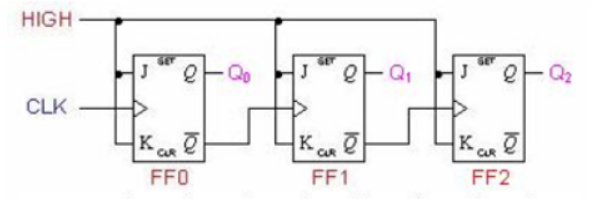


The above circuit shows the circuit diagram of a 3-bit asynchronous up counter, in which the clock pulse is given as clock input for JK FF1. For the other flip-flops, the clock input is fed from the output of previous flip-flops.

The clock pulse count is noted at the output of each flip-flop(QCQBQA), where QA is the LSB and QC is the MSB.

At the falling edge of each clock pulse, the output of JF FF1 toggles. For each logic HIGH output(QA = 1) of JK FF1, at its falling edge, JK FF2 will toggle the output(QB). Similarly, for each logic HIGH output(QB = 1) of JK FF2, JK FF3 will toggle the output(QC).

**Asynchronous 3 bit up counter [Rising edge flip flop] :**



Here rising edge flip flop are used to design a up counter

Here instead of Q , ‘Q bar’ is connected to next flip flop as clock .

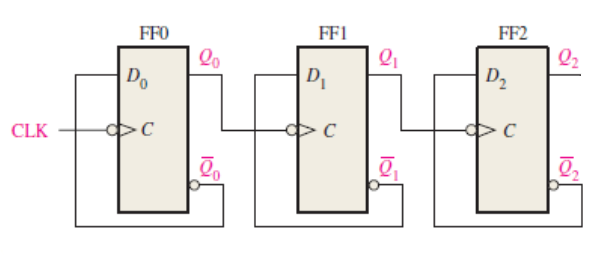
So here at rising edge of clock pulse the FF0 gets toggle For each logic HIGH output(Q0 = 1) of JK FF0, at its rising edge, JK FF1 will toggle the output(Q1). Similarly, for each logic HIGH output(Q1 = 1) of JK FF1, JK FF2 will toggle the output(Q2).

For better understanding check the timing graph which is given below at handwritten pages

**Using D flip flop :**

When D flip flops are used to design 3 bit up counter the connections are almost same except the input where instead of giving logic high(VCC) to the input(J and K) Qbar of its own D flip flop is given to the input. All other connections are same.

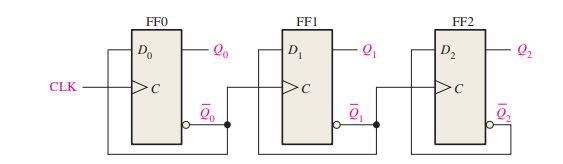
**Asynchronous 3 bit up counter [Falling edge flip flop] :**



Here 3 falling edge D flip flop are used to design a up counter

Here ‘Q bar’ is connected to the input(D) of flip flop and Q is connected to next flip flops Clock. So here at falling edge of clock pulse the FF0 gets toggle For each logic HIGH output(Q0 = 1) of JK FF0, at its falling edge, JK FF1 will toggle the output(Q1). Similarly, for each logic HIGH output(Q1 = 1) of JK FF1, JK FF2 will toggle the output(Q2).

**Asynchronous 3 bit up counter [Rising edge flip flop] :**



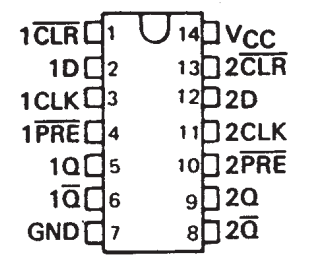
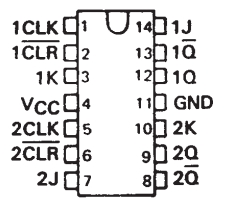
Here rising edge flip flop are used to design a up counter

Here ‘Q bar’ is connected to next flip flop as clock and also connected to the D input of its flip flop .So here at rising edge of clock pulse the FF0 gets toggle For each logic HIGH output(Q0 = 1) of JK FF0, at its rising edge, JK FF1 will toggle the output(Q1). Similarly, for each logic HIGH output(Q1 = 1) of JK FF1, JK FF2 will toggle the output(Q2).

Note : *For all circuit connections given above for clear and preset pins logic high should be given.*

**Pin diagram:**

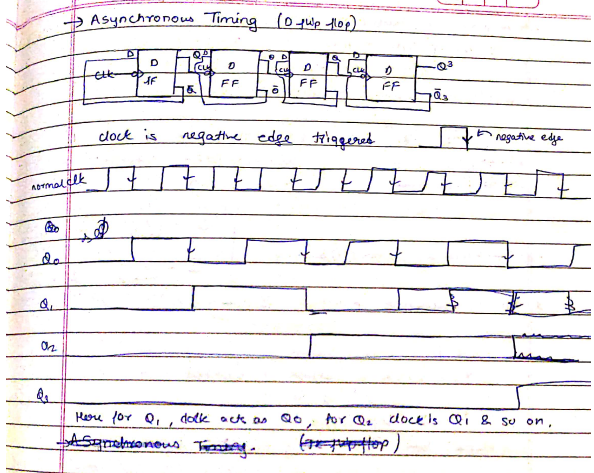
D Flip flop JK Flip flop



**Procedure:**

In practicals for 3 bit up counter we used rising edge D flip flop.

1. First take the breadboard and connect the 2 IC 7474 (D flip flop) on the breadboard.
2. Connect 1’Q bar’ to 2CLK and 2’Q bar’ to 1CLK(2nd IC) and connect the 1’Qbar’ of 2nd IC in similar fashion.
3. Now Connect 1’Q bar’ to 1D(1st IC) and 2’Q bar’ to 2D(1st IC) and connect the 1’Qbar’ of 2nd IC to 1D(2nd IC).
4. Also give VCC to all the clears(CLR) and preset(PRE) of the flip flops used.
5. Now give clock pulse to 1CLK( 1st IC) using the function generator (Also check the frequency of the clock pulse using CRO).
6. Give VCC and GND to pin 14 and pin 7 respectively.
7. Now connect the cathode of consecutive 3 LED from LED board to 1Q( 1st IC), 2Q( 1st IC), 1Q(2nd IC) respectively this is our output terminals and connect the anode(gnd) to GND.
8. Now turn on the switch of power supply(Give 5V) and the function generator(use square waves having frequency 1hz).
9. Check the whether the counter is counting from 0 to 7 and then counting in loop of 0 to 7.

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**Conclusion:**

Thus 3 bit asynchronous up counter was designed and verified.

**Citiations :**

* <https://www.geeksforgeeks.org/counters-in-digital-logic/>
* <https://www.electronics-tutorial.net/sequential-logic-circuits/asynchronous-counter/>
* Texas instruments(For pin diagram)
* Floyd Thomas